In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please amend pending claims 1-4, 6, 8, 9, 12-14, 18, 19, 23, 36, 38, 39, 41 and 42 as noted below.

1. (Currently Amended) A system for addressing unique locations in an array comprising:

a plurality of addressing layers, each addressing layer including ~~that include~~ addressable switch elements of at least two types, each type of switch element [[is]] being responsive to at least one of at least two types of switching signals; ~~capable of transmission through the addressing layers;~~

wherein a switching signal applied to an addressing layer is transmitted to all of the addressable switch elements within the addressing layer; and

a plurality of serial connections of ~~selected~~ addressable switch elements, each serial connection including one switch element from each of the plurality of addressing layers, each serial connection separately located to establish a unique array address[[es]]. ~~based on the state of the serially connected addressable switch elements.~~

2. (Currently Amended) The system of claim 1, wherein each type of addressable switch element is responsive to only one of the ~~plurality~~ at least two types of switching signal ~~types~~.

3. (Currently Amended) The system of claim 2, wherein the number of types of switch elements is exactly two, the number of switching signal types is exactly two, and a specific array location is uniquely addressed when the series of switching signals applied to the plurality of addressing layers ~~is set to a series of corresponding~~ corresponds to a unique binary number.

4. (Currently Amended) The system of claim 1, wherein a specific array location is addressed if each of the ~~series of~~ addressable switch elements in a serial connection establishing ~~connected to specify~~ said location is switched to an enabled state by [[the]] a series of switching signals applied to the plurality of addressing layers.

5. (Canceled)

6. (Currently Amended) ~~The system of claim 5,~~ A system including a plurality of uniquely addressable locations comprising:

a plurality of virtual columns, each virtual column including a plurality of serially connected switch elements, wherein each switch element of the plurality of serially connected switch elements may be one of a plurality of types responsive to at least one of a plurality of switching signal types;

wherein [[the]] serially connected switch elements of each virtual column are arranged such that a unique address for each virtual column is established; ~~and, wherein a first addressable switch element in every column is responsive to a first set of switching signals, a second addressable switch element in every column is responsive to a second particular set of switching signals.~~ and wherein the plurality of virtual columns comprises at least a first virtual column including a first switch element of a first responsive type of the plurality of types and a second switch element of a second type of the plurality of types.

7. (Original) The system of claim 6, wherein each type of addressable switch element is responsive to only one of the plurality of switching signal types.

8. (Currently amended) The system of claim 7, wherein the number of types of switch elements is exactly two, the number of switching signal types within ~~each set~~ the plurality of switching signals is exactly two, and a specific column is uniquely addressed when a series of switching ~~signals~~ signal types in the plurality of switching signal [[sets]] types represents a binary number corresponding to a uniquely addressable location.

9. (Currently amended) The system of claim 6, wherein a ~~specific~~ virtual column is addressed when each of the ~~series of addressable~~ plurality of serially connected switch elements which it includes is enabled by a ~~the plurality of~~ switching signal ~~signals~~.

10. (Original) A system for addressing unique locations in an array comprising:

a plurality of virtual columns, each virtual column including a plurality of addressable switch elements; and

at least one addressing layer coupled to at least one of the plurality of addressable switch elements.

11. (Original) The system of claim 10, wherein the plurality of addressable switch elements are selected from one of only two possible types, the first type allowing a signal to pass through the addressable switch element only upon receipt of an input of a first type, the second type allowing for a signal to pass through the addressable switch element only upon receipt of an input of a second type.

12. (Currently Amended) The system of claim 10, wherein [[the]] a virtual column is only conductive when each of the plurality of addressable switch elements in the virtual column receives an input of the type that allows for conduction through the addressable switch element.

13. (Currently Amended) The ~~device~~ system of claim 10, wherein the plurality of addressable switch elements receives an input of either the first type or the second type from an addressing layer to which it is coupled.

14. (Currently Amended) The ~~device~~ system of claim 10, wherein the plurality of addressable switch elements respond to electrical signals.

15. (Original) The device of claim 10, wherein the plurality of addressable switch elements respond to optical signals.

16. (Original) A matrix of uniquely addressable locations comprising:

a first virtual column including a first addressable switch element and a second addressable switch element;

a second virtual column including a third addressable switch element and a fourth addressable switch element.

17. (Original) The matrix of claim 16, further comprising:

a first addressing layer; and

a second addressing layer;

wherein the first addressing layer is coupled to the first addressable switch element and the third addressable switch element and wherein the second addressing layer is coupled to the second addressable switch element and the fourth addressable switch element.

18. (Currently Amended) The matrix of claim 17, wherein the first addressable switch element only allows a signal to pass through it upon receipt of an input of a first input type received from the first addressing layer and, the second addressable switch element only allows a signal to pass through it upon receipt of an input of a second input type received from the second addressing layer.

19. (Currently Amended) The matrix of claim 17, wherein the first ~~signal~~ input type is the same ~~and~~ as the second ~~signal~~ input type.

20. (Original) The matrix of claim 17, wherein the first input type is a logical high value and the second input type is logical low value.

21. (Original) The matrix of claim 17, wherein the first input type is a first wavelength of light and the second input type is a second wavelength of light.

22. (Original) The matrix of claim 17, wherein the first input type is an alternating current electrical signal having a first frequency and the second input type is an alternating current having a second frequency.

23. (Currently Amended) The matrix of claim 16, wherein the first virtual column is only conductive when the first addressable switch element receives an input of the input type that allows for transmission of a signal through the first addressable switch element and the second addressable switch element receives an input that allows for transmission of a signal through the second addressable switch element.

24. (Original) The matrix of claim 16, wherein the first addressable switch element responds to electrical signals.

25. (Original) The matrix of claim 16, wherein first addressable switch element responds to optical signals.

26. (Original) A matrix of uniquely addressable locations comprising:

two or more addressing multi-layers, the addressing multi-layers including two or more sub-layers for conducting an addressing signal; and

a plurality of virtual columns, the virtual columns including a plurality of addressable switch elements coupled to the two or more of the addressing multi-layers.

27. (Original) The matrix of claim 26, wherein the plurality of addressable switch elements is enabled by a sub-set of the sub-layers which it is associated with.

28. (Original) The matrix of claim 27, wherein the addressing multi-layers include only two sub-layers and, wherein the addressable switch elements are enabled by a signal received from only one of the sub-layers.

29. (Original) The matrix of claim 28, further comprising:

means for switching an address signal associated with one of the plurality of addressing multi-layers to one of the two sub-layers.

30. (Original) A matrix of discretely addressable locations comprising:

an optically conductive material;

a plurality of virtual columns, each including at least two addressable switch elements, the virtual columns being disposed in the optically conductive material; and

a first signal generator that generates at least two different optical signals, the generator being disposed such that it produces at least one optical signal that passes through the optically conductive material.

31. (Original) The matrix of claim 30, wherein at least two of the addressable switch elements become conductive only in response to one of the at least two different optical signals.

32. (Original) The matrix of claim 31, wherein at least one of the plurality of virtual columns is conductive if both of the addressable switch elements of that column are in a conductive state.

33. (Original) The matrix of claim 32, further comprising:

a second signal generator that generates at least two different optical signals, the generator being disposed such that the it produces at least one optical signal that passes through the optically conductive material.

34. (Original) The matrix of claim 30, wherein at least one of the plurality of virtual columns includes a data storage element.

35. (Original) The matrix of claim 30, wherein at least one of the plurality of virtual columns is coupled to a data storage element.

36. (Currently Amended) A matrix of uniquely addressable locations comprising:

a plurality of addressing layers having a first portion of a first type and a second portion of a second type, the first portion allowing a signal to pass there-through only upon ~~the~~ receipt of a first signal type and the second portion allowing a signal to pass there-through only upon ~~the~~ receipt of a second signal type;

wherein at least two of the plurality of addressing layers are disposed such that an ordered alignment of the first and second portions of ~~the~~ at least two of the ~~two or more~~ addressing layers is established.

37. (Original) The matrix of claim 36, wherein a second addressing layer is disposed over a first addressing layer such that a sub-portion of each of the portions of the second addressing layer is superposed over a sub-portion of the portions of the first addressing layer.

38. (Currently Amended) The matrix of claim 36, wherein each of the two portions of the first and second ~~address~~ addressing layers is divided into non-contiguous regions.

39. (Currently Amended) The matrix of claim 37, wherein the plurality of addressing layers are arranged to overlie one another such that sub-portions of at least the first and second addressing layers result in unique serial transverse positioning combinations of portion types resulting in regions within the plurality of addressing layers having unique addresses.

40. (Original) The matrix of claim 36, wherein the first and second signal types are optical signals or electrical signals.

41. (Currently Amended) The matrix of claim 36, wherein a portion of a second addressing layer is arranged such that it overlies at least a portion of the first portion of a first addressing layer in a substantially perpendicular manner.

42. (Currently Amended) The matrix of claim 41, wherein the second addressing layer includes a third portion and a fourth portion, the third portion allowing a signal to pass

there through only upon ~~the~~ receipt of the first ~~input~~ signal type, the fourth portion allowing a signal to pass there through only upon receipt of the second ~~input~~ signal type.

43. (New) The system of claim 6, further comprising a second virtual column of serially connected switch elements wherein all the serially connected switch elements of the second virtual column are of the first responsive type.

44. (New) The system of claim 43, further comprising a third virtual column of serially connected switch elements wherein all the serially connected switch elements of the third virtual column are of the second responsive type.